

JMV5772ND

Product Preview

40V N-Channel MOSFET

Features

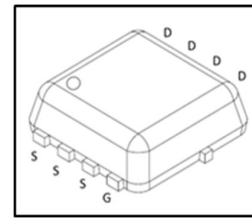
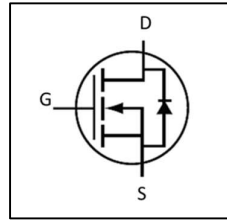
- Advanced shielded-gate technology
- Ultra-low on-resistance and gate-charge
- RoHS compliant
- 100% avalanche tested



Product Summary	
V _{DS}	40V
R _{DS(ON)}	2.8 mΩ (Typ.)
	3.4 mΩ (Max.)

Applications

- Motor controllers
- DC-to-DC convertors
- Battery-driven electronic products, electrical equipment and machines


Ordering Information

Part Number	Marking	Package	Packaging
JMV5772ND	V5772ND	DFN3.3x3.3	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Drain-to-Source Voltage	V_{DS}	40	V
Gate-to-Source Voltage	V_{GS}	± 20	
Continuous Drain Current, Silicon Limited ($T_C = 25^\circ\text{C}$) ⁽¹⁾	I_D	99	A
Continuous Drain Current, Silicon Limited ($T_C = 100^\circ\text{C}$) ⁽¹⁾	I_D	63	
Continuous Drain Current, Silicon Limited t ($T_A = 25^\circ\text{C}$) ^{(2), (3)}	I_D	22	
Continuous Drain Current, Silicon Limited ($T_A = 100^\circ\text{C}$) ^{(2), (3)}	I_D	14	
Pulsed Drain Current ⁽⁴⁾	I_{DM}	200	
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	56.8	W
Linear Derating Factor	-	0.45	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ⁽⁵⁾	E_{AS}	90 ⁽⁶⁾	mJ
Avalanche Current ⁽⁷⁾	I_{AS}	28	A
Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	

Thermal Characteristics

Parameter	Symbol	Max	Unit
Junction-to-Ambient Thermal Resistance ⁽³⁾	$R_{\theta JA}$	45	$^\circ\text{C}/\text{W}$
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	2.2	

Static Electrical Characteristics ⁽⁸⁾

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	40	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.1	-	2.2	
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	-	2.8	3.4	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$	-	3.8	4.9	m Ω

Dynamic Electrical Characteristics ⁽⁸⁾

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward Transconductance	g_{fs}	$V_{DS} = 5V, I_D = 20A$	-	72	-	S
Total Gate Charge	Q_g	$V_{GS} = 10V,$ $V_{DS} = 20V,$ $I_D = 20A$	-	22.9	-	nC
Gate-to-Source Charge	Q_{gs}		-	3.1	-	
Gate-to-Drain Charge	Q_{gd}		-	3.8	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V,$ $V_{DS} = 20V,$ $I_D = 20A,$ $R_G = 3.0\Omega$	-	TBC	-	ns
Rise Time	t_r		-	TBC	-	
Turn-Off Delay Time	$t_{d(off)}$		-	TBC	-	
Fall Time	t_f		-	TBC	-	
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $f = 1MHz,$ $V_{DS} = 20V$	-	1802	-	pF
Output Capacitance	C_{oss}		-	716	-	
Reverse Transfer Capacitance	C_{rss}		-	84	-	

Diode Characteristics ⁽⁸⁾

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 20A$	-	0.8	-	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0V, I_S = 20A,$ $di_S/dt = 100A/\mu s$	-	47	-	ns
Reverse Recovery Charge	Q_{rr}		-	36	-	nC

- (1) Rated according to $R_{\theta JC}$
- (2) Rated according to $R_{\theta JA}$
- (3) Surface-mounted on 1 inch² FR4 board, 2 oz Cu
- (4) Limited by maximum T_J
- (5) Starting $T_J = 25^\circ C, L = 0.1mH, V_{DD} = 30V, V_{GS} = 10V$
- (6) TBC: To be confirmed
- (7) Pulse width limited by maximum T_J
- (8) $T_J = 25^\circ C$ unless otherwise specified

Typical Electrical Characteristics

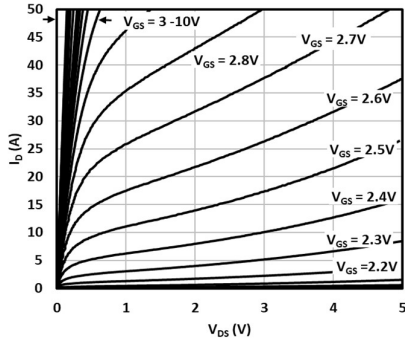


Fig. 1 Output characteristics

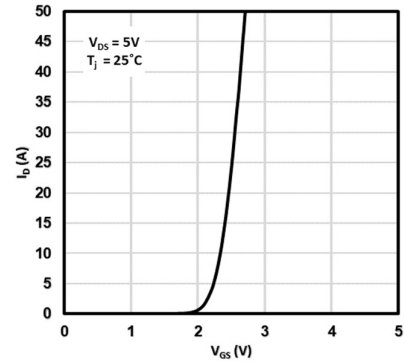


Fig. 2 Transfer characteristics

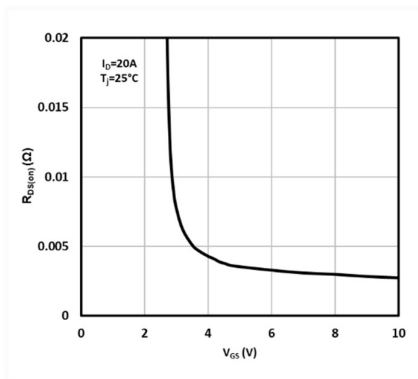


Fig.3 On-resistance vs. gate voltage

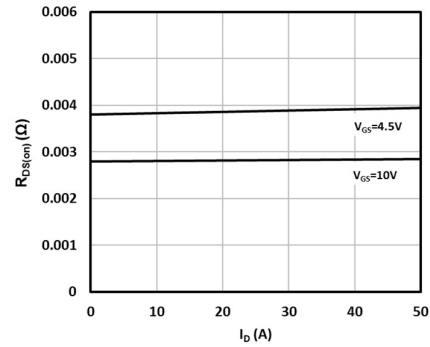


Fig.4 On-resistance vs. drain current

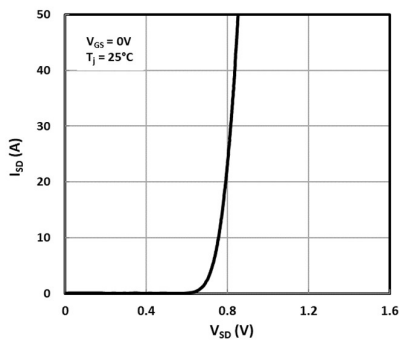


Fig.5 Source-to-drain diode forward characteristics

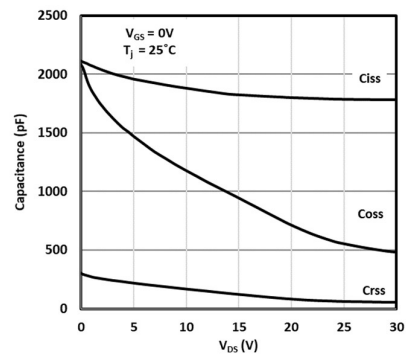
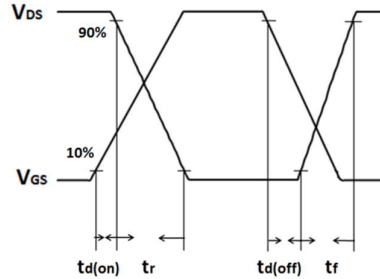
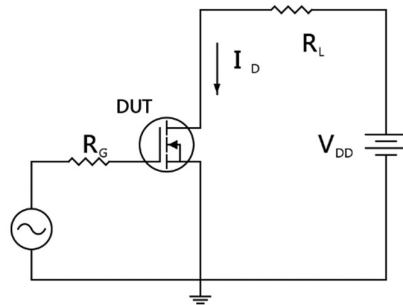
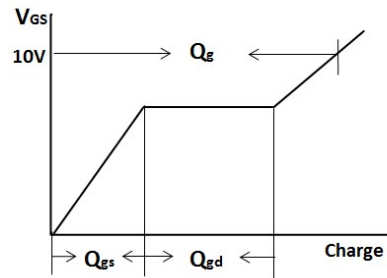
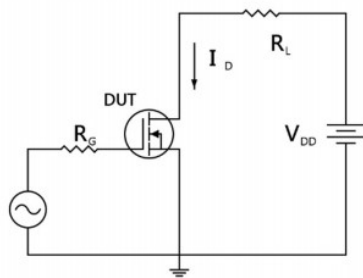


Fig.6 Capacitance vs. drain-to-source voltage

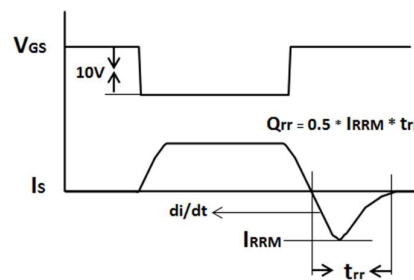
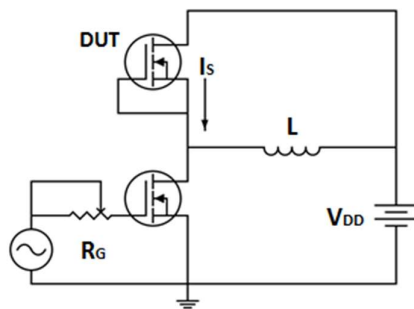
Test Circuits and Waveforms



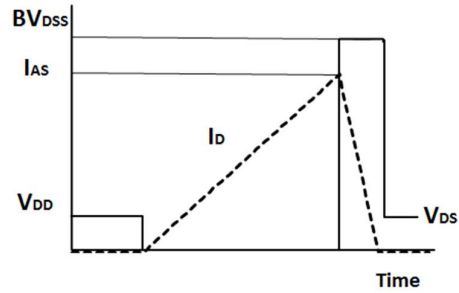
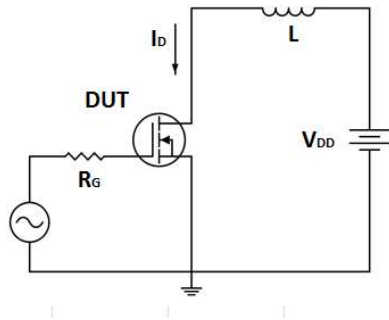
Resistive switching time test circuit & waveforms



Gate charge test circuit & waveform

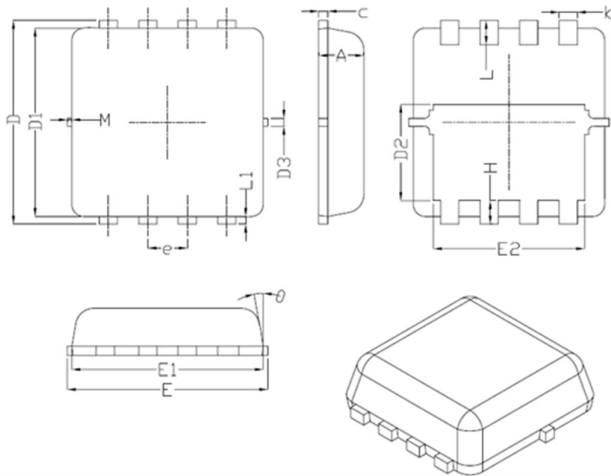


Peak diode recovery dv/dt test circuit & waveforms



Unclamped inductive switching test circuit & waveforms

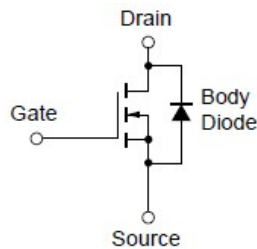
Package Drawing



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
b	0.25	0.32	0.39
c	0.10	0.15	0.25
D	3.00	3.30	3.60
D1	3.00	3.10	3.50
D2	1.48	2.00	2.20
D3	--	0.20	--
E	3.00	3.30	3.60
E1	3.00	3.10	3.25
E2	2.29	2.49	2.69
e	0.65 BSC		
H	0.15	0.25	0.50
L	0.15	0.40	0.60
L1	0.05	0.15	0.25
α	8°	10°	12°
M	--	0.10	--

DFN 3.3x3.3

Equivalent Circuit



Revision history of JMV5772ND specification

Version	Change Items	Effective Date
1.00	Initial Release	11-Jun-21

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